**REMARKS**

Claims 1-7 are rejected under 35 U.S.C. 102(e), as anticipated by Iijima US Pub. #2002/0118570.

**1. Introduction to the amended specification:**

Table 1, whose detailed description is originally shown in paragraph [0023], was lost in the original specification of the present application due to some unknown reasons. Therefore, the missing Table 1 is added in the above AMENDMENTS TO THE SPECIFICATION section, and no new matter is introduced. Allowance of the amended specification is hereby requested.

**2. Objection to the drawings:**

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a "method for reading a non-volatile memory with multi-level … the fourth programming states" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

**Response:**

The missing Table 1 is added in the above AMENDMENTS TO THE SPECIFICATION section, and Table 1 shows the features disclosed in the claims. No new matter is

introduced. Allowanc of the present application is hereby requested.

**3. Rejection of claims 1-7 under 35 U.S.C. 102(e):**

Figure 6 or 15 of Iijima is directed to a method for reading a nonvolatile memory with multi-level output currents comprising applying a first reading voltage (2.5V) on a conductor (word line) of the memory cell (MC1); applying a second reading voltage (5V or 2V) on a drain of the memory cell; and grounding (0V) a source (a paragraph [0014] or [0063]) of the memory cell, thereby obtaining an output current; wherein the output current comprises a maximum output current (11 state, fig.15) corresponding to the memory cell in the first programming state, a first output current corresponding to the memory cell in the second programming state (10 state, fig.15), a second output current corresponding to the memory cell in the third programming state (01 state, fig.15), and a third output current corresponding to the memory cell in the fourth programming state (00 state, fig.15).

**Response:**

First, the amended claim 1 is amended according to the specification of page 5, lines 32-34. No new matter is introduced.

Second, the Applicants intend to point out the difference between the amended claim 1 of the present application and Iijima's disclosure. The amended claim 1 of the present application is repeated below:

"1.A method for reading a non-volatile memory with multi-level output currents comprising:

providing a memory cell;

applying a first reading voltage on a conductor of the memory cell;

applying a second reading voltage on a drain of the memory cell; and

grounding a source of the memory cell, thereby obtaining an output current;

wherein **the memory cell comprises a first programming state, a second programming state, a third programming state, or a fourth programming state,** and **the output current comprises a maximum output current corresponding to the memory cell in the first programming state, a first output current corresponding to the memory cell in the second programming state, a second output current corresponding to the memory cell in the third programming state, or a third output current corresponding to the memory cell in the fourth programming state."**

As described in the amended claim 1, there are four kinds of memory cells 10, and each kind of memory cells 10 stores a binary value, such as 11, 10,01, or 00. That is, **a binary value, such as 11, 10,01, or 00, is detected according to <u>an output current of one memory cell 10</u>. Accordingly, a binary value, such as 11, 10, 01, or 00, is detected through <u>reading only one memory cell 10</u>.**

However, Iijima discloses that the multileveled data retained in the multilevel memory cell is detected

according to the total amount of the memory c ll currents flowing through the first memory cell MC1 and the second memory cell MC2 in the multilevel memory cell (paragraph [0118], and Figs.13-15). That is to say, **a binary value, such as 11, 10,01, or 00, is detected according to the total amount of output currents flowing through the first memory cell MC1 and the second memory cell MC2**. Accordingly, **a binary value, such as 11, 10,01, or 00, is detected through simultaneously reading the first memory cell MC1 and the second memory MC2**. Therefore, the method taught in the present application should be definitely different from that disclosed in Iijima's disclosure. Reconsideration of the claim 1 is hereby requested.

As claims 2-7 are dependent upon the amended claim 1, they should be allowed if the amended claim 1 is allowed. Reconsideration of the claims 2-7 is hereby requested.

Sincerely yours,

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